OPTIMAL CAD OF MESFETS FREQUENCY MULTIPLIERS WITH AND WITHOUT FEEDBACK

C. GUO* - E. NGOYA* - R. QUERE* - M. CAMIADE** - J. OBREGON*

* I.R.C.O.M. Université de Limoges - CNRS 87060 LIMOGES CEDEX - FRANCE
** THOMSON Hybrides et Microondes/DHM, 29 Avenue Carnot, 91300 MASSY - FRANCE

ABSTRACT

In this paper, we propose a method to derive the optimal operating-conditions of a given MESFET to obtain an optimum frequency multiplier. The key point of this approach is that no topology of the embedding network is to be chosen "a priori". The optimum bias voltages and the optimum load impedances (including possible feedback circuit) are found as results of the method.

This new method allows to know the ultimate performances that can be achieved by a given device working as frequency multiplier.

I - INTRODUCTION

One of the major problems of frequency multiplier's designers is to determine the optimum operating-conditions {1} {2}, i.e : bias voltages, load impedances (including possible feedback circuit) at all frequencies (input fundamental frequency ω_0, output frequency $N\omega_0$, and idler frequencies $i\omega_0$, $i \neq 1, N,$) in order to obtain maximum power at frequency $N\omega_0$ for a minimum input power.

Today this is usually done by a "cut and try" non-linear simulation which is executed by first fixing "a priori" a topology of the embedding circuit and then varying the linear elements and device bias-voltages to obtain an "optimum" characteristic. But can the fixed topology provide the achievable limit for the device? Are the load impedances (or possibly the output-input feedback circuit) optimized for all frequencies ? Clearly, is the device behaviour globally optimized ?

In this paper, we propose a method to derive the optimal operating-conditions of a given MESFET to obtain an optimum frequency multiplier. The key point of this approach is that no topology of the embedding network is to be chosen "a priori". The method allows to find: the optimum bias voltages; the optimum load impedances, including possible feedbacks.

This method allows to know the ultimate performances that can be achieved by a given device working as frequency multiplier.

II - FORMULATION OF THE OPTIMIZATION PROBLEM

Given a field effect transistor defined by a non-linear model, let us derive the optimal operating-conditions of a multiplier to obtain the maximum output power at $N\omega_0$ for a minimum input power at fundamental frequency ω_0.

In mathematical form, the non-linear device model describes the functional relationships between dependent and independent port-variables (see Fig. 1). However it is well known that the dependent variables in a FET are in fact functions of $v_{gs}(t)$ and $v_{ds}(t)$ (see Fig. 1). So we can write :

$$\begin{cases} i_1(t) = F_{NL}(v_{gs}(t), v_{ds}(t)) \\ i_2(t) = F_{NL}(v_{gs}(t), v_{ds}(t)) \end{cases} \quad (1)$$

From these equations, it is clear that the behaviour of the device is completely defined by the knowledge of the independent variables $v_{gs}(t)$ and $v_{ds}(t)$.

Let us consider that the device model is driven by a frequency ω_0. Harmonic frequencies $i\omega_0$ ($i = 2, 3, \ldots, N, \ldots$) are generated by the non linear device. Voltages at gate and drain of the FET may be expanded in Fourier series :

0149-645X/88/0000-1115$01.00 © 1988 IEEE

$$v_{gs}(t) = V_{gs0} + \sum_{l=1}^{L} V_{gsl}\cos(l\omega_0 t + \Psi_l)$$
$$v_{ds}(t) = V_{ds0} + \sum_{l=1}^{L} V_{dsl}\cos(l\omega_0 t + \theta_l) \quad (2)$$

If the device is used as frequency multiplier, we define that the input frequency is the fundamental frequency ω_0 and the output frequency is $N\omega_0$ (where N is the multiplication factor).

Introducing equation (2) in (1), and taking the Fourier transform of $i_1(t)$ and $i_2(t)$, we obtain the Fourier coefficient vectors of dependent variables : I_1, I_2.

Defining now the maximum output power of the FET at $N\omega_0$ for a minimum input power as the desired feature, we may write the function to be optimized as :

$$P(\vec{V}_{gs}, \vec{V}_{ds}) = -\mathrm{Re}\{\vec{V}_{2N}\cdot\vec{I}^*_{2N} + \vec{V}_{1N}\cdot\vec{I}^*_{1N}\} - \{\mathrm{Re}\,\vec{V}_{11}\cdot\vec{I}^*_{11}\} \quad (3)$$

where $P(\vec{V}_{gs}, \vec{V}_{ds})$ is called the added power of the multiplier.

During the optimization iterative process, the variables are subject to the constraints {3}. That is : their variations are limited by conditions allowing their physical realizabilities. These constraints are derived from activity and passivity considerations of the active-device ports.

Once optimization is achieved, optimum voltages and currents V_1, V_2, I_1, I_2 at fundamental and harmonic frequencies are known, optimum loads and bias voltages may be then deduced.

III - PHYSICAL EXPLANATION OF THE MULTIPLICATION PROCESS IN A MESFET

In order to understand the behaviour of FETs operating as a frequency multipliers, let us consider the simplified model shown in Fig. 2 and its corresponding characteristics. The limiting curves indicate the limits that cannot be exceeded by the gate voltage V_ϕ, the drain voltage V_{dsmax} and the drain current I_{dmax}. These limitations are due to the input Schottky diode and avalanche breakdown between gate and drain.

The frequency multiplication may be explained as follows, (see Fig.3): A sinusoidal gate voltage at ω_0, gives a drain current pulse I_d which may be decomposed analytically in Fourier series. The drain current component I_N at the output frequency $N\omega_0$ is a function of the gate conduction angle $2\theta_g$ (Fig. 3) and may be optimized as shown in Fig. 4. This figure 4 represents I_N as a function of $2\theta_g$ and θ_{gopt} as a function of N. It may be shown that θ_{gopt} is equal to $120°/N$ and I_N/I_{dmax} equal approximately to $0.54/N$ $(N > 1)$

Knowing now θ_{gopt} and the characteristic $I_d = f(V_{gs}, V_{ds})$ shown in Fig. 3, the optimum gate bias voltage V_{gs0} and the fundamental frequency component V_{gs1} can be deduced. On the other hand, from Fig. 5 the maximum peak to peak drain voltage at output frequency $N\omega_0$ is given by $2V_{Nopt} = V_{dsmax} - V_{dsmin}$ and the drain bias voltage $V_{ds0} = (V_{dsmax} + V_{dsmin})/2$. Finally the output load at $N\omega_0$ is given by $G_{opt}(N\omega_0) = I_{Nopt}/V_{Nopt}$ This load is generally made by a parallel turned circuit at $N\omega_0$. Fig. 5 indicates the drain load locus for a MESFET working as a doubler loaded by a pure conductance at $2\omega_0$ and a short circuit at other frequencies.

Note that in the plane : $I_d = f(V_{gs}, V_{ds})$, the optimum load is necessarily a conductance since it is that load which needs the minimum swing of v_{ds} for a given output power.

Let us consider the role played by a feedback circuit in a frequency multiplier {4}. It is clear from Fig.3 that a feedback from drain to gate allows to combine a harmonic voltage component with fundamental sinusoidal input voltage in the gate. The result makes a non sinusoidal gate voltage. This total voltage gives a drain current pulse with an enhanced component I_N at desired output frequency $N\omega_0$.

IV - OPTIMIZATION RESULTS

The device used in our example is a 0.5*800 µm GaAs MESFET {5}. Fig.1 shows the equivalent circuit.

The optimization gives the maximum added-power P_{add} :

$$P_{add} = \frac{1}{2}\mathrm{Re}\{-\vec{V}_{22}\vec{I}^*_{22} - \vec{V}_{12}\vec{I}^*_{12}\} - \frac{1}{2}\mathrm{Re}\{\vec{V}_{11}\vec{I}^*_{11}\} \quad (4)$$

Under the physical realizability constraints :

$$\mathrm{Re}\{\vec{V}_{1j}\vec{I}^*_{1j}\} + \mathrm{Re}\{\vec{V}_{2j}\vec{I}^*_{2j}\} \geq 0 \quad j=2,\ldots,N,\ldots \quad (5)$$

(the transistor acts as a generator at $j\omega_0$) ;

and $\mathrm{Re}\{\vec{V}_{11}\vec{I}^*_{11}\} > 0$ (6)

(The transistor presents a passive impedance to the input generator at ω_0).

Two frequency doublers have been optimized : a 10 to 20 GHz "low

frequency" doubler, and a 20 to 40 GHz "millimetric" doubler.

- Low frequency doubler :

In this example, a feedback at frequency $2\omega_0$ is needed to obtain the maximum added - power. In order to compare the influence of the feedback, we have performed another optimisation for the same transistor at same frequencies, constrained to work without feedback circuit. Table 1 shows the comparisons. Fig. 6 represents the dynamic current - voltage trajectory in the I_d - V_{ds} plane for the doubler with feedback.

- Millimetric doubler :

The optimum power at $2\omega_0$ (40 GHz) is obtained at gate port of the MESFET. This is because for high operating frequencies the internal feedback of the MESFET equivalent circuit is important. The best result in this case is obtained without external feedback.

P = 22 dBm at 20 GHz

P = 16 dBm at 40 GHz

The optimization results show that the influence of higher harmonics ($i > 3$) is very small. However, the effect of feedback is very important for a MESFET doubler when the transistor has gain at the frequency $2\omega_0$.

To confirm the validity of the proposed optimization method, the optimized impedances have been synthetized and resulting multipliers have been analyzed in a Harmonic Balance circuits simulator. Varaitions of the load impedances have shown that the doublers were in their optimum state. After these confirmations, two doublers have been realized.

Fig. 7 represents a 10 to 20 GHz doubler without feedback. The optimum output power at 20 GHz is 16 dBm. Fig.8 shows the output power at $2\omega_0$ in fonction of input power at ω_0. The experimental result shows a correlation better than 1.8 dB.

V - CONCLUSION

In this paper, we propose a new method of designing optimum frequency multipliers. Using this method, the ultimate capability of a given MESFET working as frequency multiplier is determined.

The method has been applied to design doublers at low frequencies from 10 to 20 GHz and at millimeter-wave from 20 to 40 GHz. Experimental doublers are under measurement, first results have given good agreement with theoretical predictions.

REFERENCES

{1} **A. GOPINATH, J.B. RANKIN**
"Single-gate MESFET frequency doublers"
IEEE Trans. Microwave Theory, Tech., Vol.MTT-30, n°6, June 1982, pp.869-875

{2} **R. GILMORE**
"Concepts in the design of frequency multipliers"
Microwave Journal, March 1987, pp.129-139

{3} **M.C. ALBUQUERQUE, C. GUO and J. OBREGON**
"A new approach to fundamental frequency analysis ans optimization of non-linear microwave circuit"
15 th E.M.C., pp.515-520

{4} **C. RAUSCHER**
"High-frequency doubler operation of GaAs Field-effect transistors"
IEEE Trans. Microwave Theory Tech., Vol.MTT-31, n°6, June 1983, pp.462-473

{5} **C. GUO, M. CAMIADE, D. ROUSSET, A. CESSEY, J. OBREGON and A. BERT**
"Optimum design of non-linear power FET amplifiers"
IEEE Trans. Microwave Theory Tech., Vol.MTT-35, n°12, December 1987, PP.1348-1354

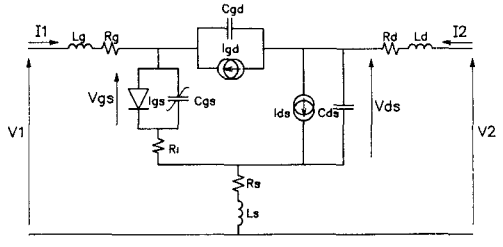

Figure 1 : Non linear FET model

without feedback			with feedback		
Pin(dBm)	Pout(dBm)	Padded(dBm)	Pin(dBm)	Pout(dBm)	Padded(dBm)
13.8	17.8	15.6	11.0	18.2	17.3

Table : Comparisons of doublet with and without feedback.

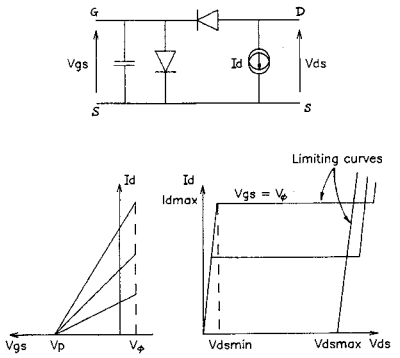

Figure 2 : Simplified non linear FET model

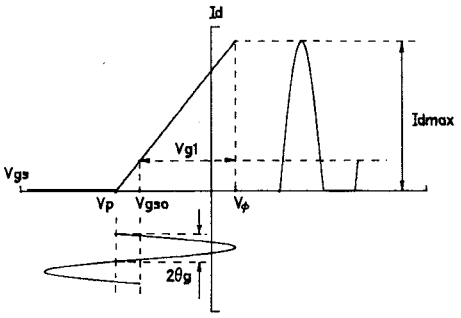

Figure 3 : Output wareshape for the circuit of Fig. 2 and Fourier component of the drain current at $N\omega_o$.

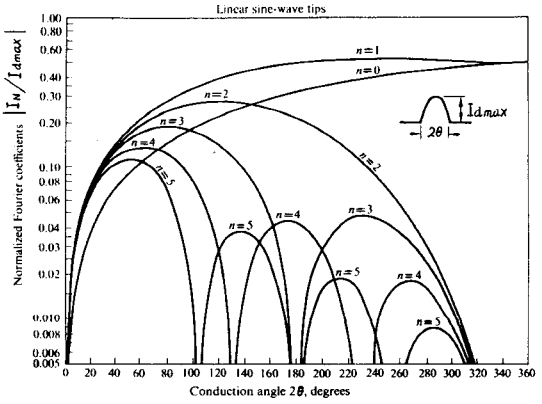

Figure 4 : Normalized amplitude of I_N function of the conduction angle.

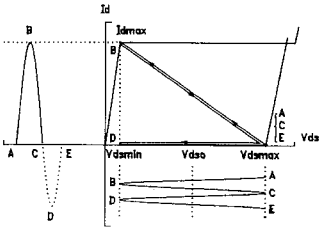

Figure 5 : Graphical explanation of a MESFET frequency doubler

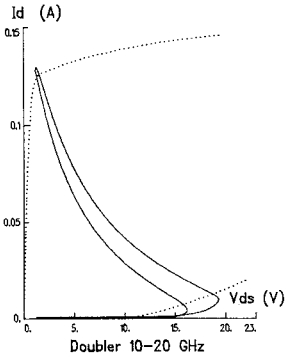

Figure 6 : Dynamic current-voltage trajectory in the I_d-V_{ds} plane for the doubler with feedback

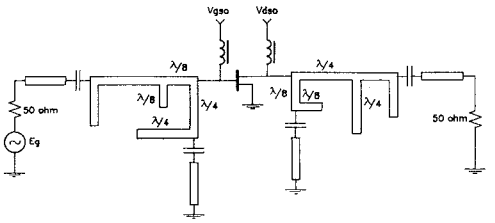

Figure 7 : 10 to 20 GHz frequency doubler without feedback.

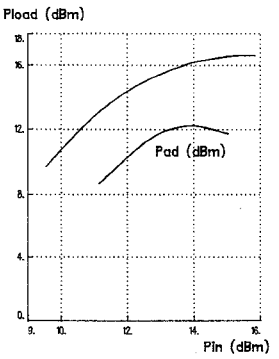

Figure 8 : Output power at 20 GHz as frequency doubler shown input power.